

Low power consumption, Low ESR Cap. Compatible AS7125L Series

General Description

AS7125L series are highly precise, low power consumption, positive voltage regulators manufactured using CMOS technologies .The series provides large currents with a significantly small dropout voltage.

The series is compatible with low ESR ceramic capacitors .The current limiter's foldback circuit also operates as a short protect for the output current limiter and the output pin.

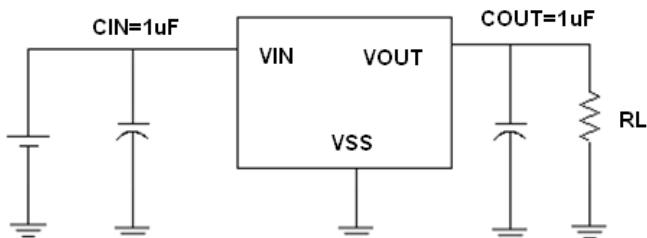
Features

- Highly Accurate: $\pm 1\%$
- Output voltage range: 1.0V~5.0V
- Low power consumption: 4uA(TYP.)
- Large output current: 300mA ($V_{IN}=4.3V, V_{OUT}=3.3V$)
- Input voltage: up to 6 V
- Dropout voltage:
0.11V at 100mA and 0.24V at 200mA
- Excellent Input Stability
- Be available to regulator and reference voltage
- Packages: SOT23

Typical Application

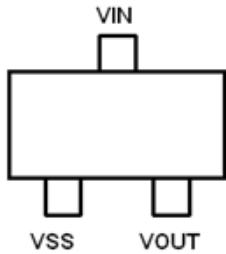
- Battery powered equipment
- Communication tools
- Mobile phones
- Portable games
- Portable AV systems
- Cameras, Video systems
- Reference voltage source

Typical Application Circuit



Pin Configuration

SOT23



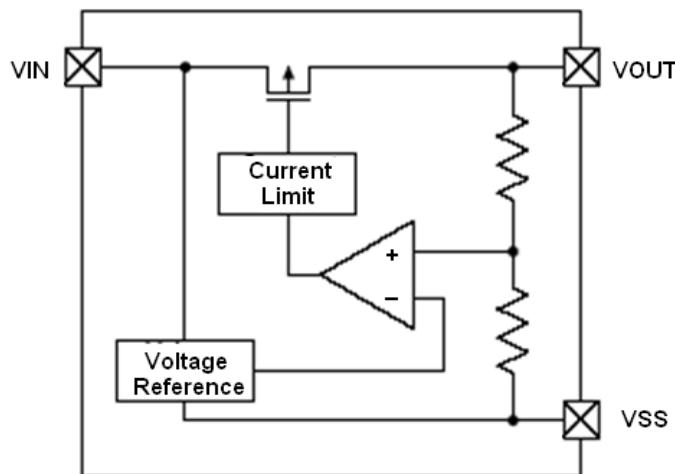
Pin Assignment

Pin	Name	Function
1	VSS	Ground
2	VOUT	Output
3	VIN	Input

Absolute Maximum Ratings

Parameter	Symbol	Description	Units
Input Voltage	V_{IN}	6.5	V
Output Current	I_{OUT}	390	mA
Output Voltage	V_{OUT}	$V_{SS}-0.3 \sim V_{OUT}+0.3$	V
Power Dissipation	P_d	300	mW
Operating Ambient Temperature	T_{Opr}	-25 ~ +85	°C
Storage Temperature	T_{stg}	-40 ~ +125	°C

Block Diagram



Electrical Characteristics

($V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=1\mu F$, $T_a=25^{\circ}C$ Unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIX	TYP	MAX	UNIT
Output Voltage	$V_{OUT}(E)$ (Note 2)	$I_{OUT}=10mA$, $V_{IN}=V_{OUT}+1V$	X 0.99	$V_{OUT}(T)$ (Note 1)	X 1.01	V
Input Voltage	V_{IN}				6	V
Maximum Output Current	I_{OUT} (max)	$V_{IN}=V_{OUT}+1V$		300	350	mA
Load Regulation	ΔV_{OUT}	$V_{IN}=V_{OUT}+1V$ $1mA \leq I_{OUT} \leq 100mA$		9	18	mV
Dropout Voltage (Note 3)	V_{dif1}	$I_{OUT}=80mA$		100	120	mV
	V_{dif2}	$I_{OUT}=200mA$		240	260	mV
Supply Current	I_{SS}	$V_{IN}=V_{OUT}+1V$		4	8	μA
Line Regulations	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \cdot V_{OUT}}$	$I_{OUT}=40mA$ $V_{OUT}+1V \leq V_{IN} \leq 6V$		0.07	0.2	%/V
Power Supply Ripple Rejection Ratio	PSRR	$V_{in}=[V_{OUT}+1]V$ +1Vp-pAC $I_{OUT}=10mA, f=1kHz$		50		dB
Short Circuit Current	I_{short}	$V_{in}=V_{OUT}(T)+1V$ $V_{OUT}=V_{SS}$		30	60	mA
Over Current Protection	I_{limit}	$V_{IN}=V_{OUT}+1V$		420	450	mA

Note :

1. $V_{OUT}(T)$: Specified Output Voltage

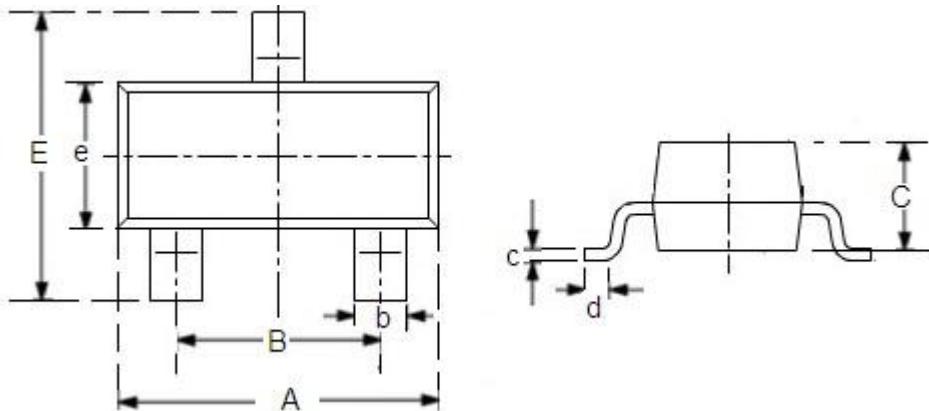
2. $V_{OUT}(E)$: Effective Output Voltage (i.e. The output voltage when " $V_{OUT}(T)+1.0V$ " is provided at the V_{in} pin while maintaining a certain I_{OUT} value.)

3. V_{dif} : $V_{IN1}-V_{OUT}(E)$

V_{IN1} : The input voltage when $V_{OUT}(E)$ appears as input voltage is gradually decreased.

$V_{OUT}(E)'$ = A voltage equal to 98% of the output voltage whenever an amply stabilized I_{OUT} ($V_{OUT}(T)+1.0V$) is input.

Packaging Information





深圳市全智芯科技有限公司
SHENZHEN ASCHIP TECH CO., LTD.

LDO
AS7125L

DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	2.7	3.1	0.1063	0.122
B	1.7	2.1	0.0669	0.0827
b	0.35	0.5	0.0138	0.0197
C	1.0	1.2	0.0394	0.0472
c	0.1	0.25	0.0039	0.0098
d	0.2	-	0.0079	-
E	2.1	2.64	0.0827	0.1039
e	1.2	1.4	0.0472	0.0551